

OptiMOS[®] -T Power-Transistor



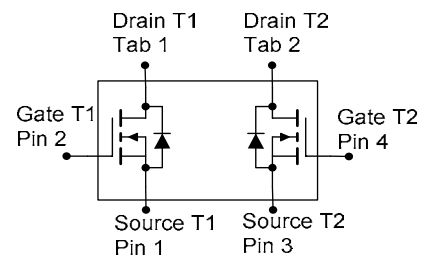
Features

- Dual N-channel Logic Level - Enhancement mode
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green Product (RoHS compliant)
- 100% Avalanche tested

Product Summary

V_{DS}	55	V
$R_{DS(on),max}^{5)}$	35	mΩ
I_D	20	A

P-TDSON-8-4



Type	Package	Marking
IPG20N06S3L-35	PG-TDSON-8-4	3N06L35

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current one channel active	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	20	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	15.5	
Pulsed drain current ²⁾ one channel active	$I_{D,pulse}$	-	80	
Avalanche energy, single pulse ^{2, 5)}	E_{AS}	$I_D=10\text{ A}$	55	mJ
Avalanche current, single pulse ⁵⁾	I_{AS}	-	20	A
Gate source voltage ⁴⁾	V_{GS}	-	±16	V
Power dissipation one channel active	P_{tot}	$T_C=25\text{ °C}$	30	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}	-	-	-	5	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint	-	100	-	
		6 cm ² cooling area ³⁾	-	60	-	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=15\text{ }\mu\text{A}$	1.2	1.7	2.2	
Zero gate voltage drain current ⁵⁾	I_{DSS}	$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=55\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current ⁵⁾	I_{GSS}	$V_{GS}=16\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance ⁵⁾	$R_{DS(on)}$	$V_{GS}=5\text{ V}, I_D=7\text{ A}$	-	53	62	m Ω
		$V_{GS}=10\text{ V}, I_D=11\text{ A}$	-	30	35	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance ⁵⁾	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	1330	1730	pF
Output capacitance ⁵⁾	C_{oss}		-	170	220	
Reverse transfer capacitance ⁵⁾	C_{rss}		-	160	240	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=27.5\text{ V},$ $V_{GS}=10\text{ V}, I_D=20\text{ A},$ $R_G=25\ \Omega$	-	3	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	8	-	
Fall time	t_f		-	9	-	

Gate Charge Characteristics^{2, 5)}

Gate to source charge	Q_{gs}	$V_{DD}=11\text{ V}, I_D=20\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	7	9	nC
Gate to drain charge	Q_{gd}		-	3	4.5	
Gate charge total	Q_g		-	18	23	
Gate plateau voltage	$V_{plateau}$		-	5.1	-	V

Reverse Diode

Diode continuous forward current ²⁾ one channel active	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	20	A
Diode pulse current ²⁾ one channel active	$I_{S,pulse}$		-	-	80	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=20\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	1.0	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=27.5\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	10	-	ns
Reverse recovery charge ^{2, 5)}	Q_{rr}		-	10	-	nC

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 5\text{ K/W}$ the chip is able to carry 22A at 25°C.

²⁾ Specified by design. Not subject to production test.

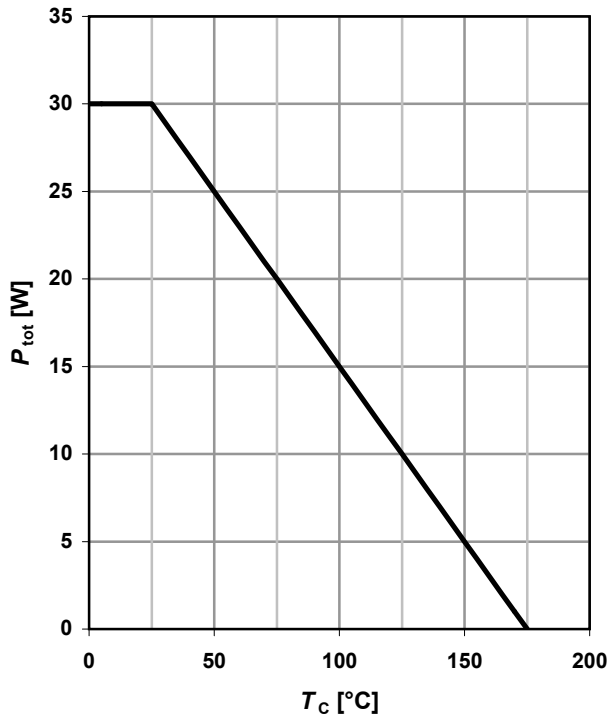
³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁴⁾ Qualified at -5V and +16V.

⁵⁾ Per channel

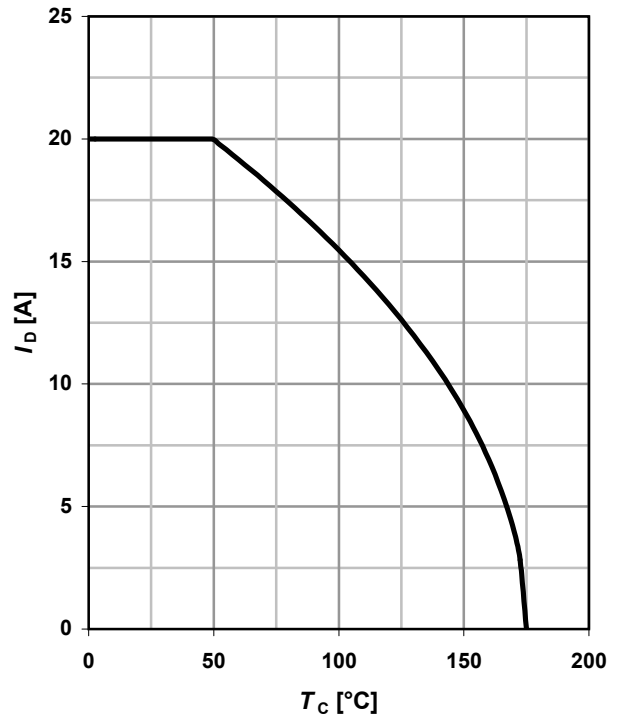
1 Power dissipation

$P_{tot} = f(T_C)$; $V_{GS} \geq 6\text{ V}$; one channel active



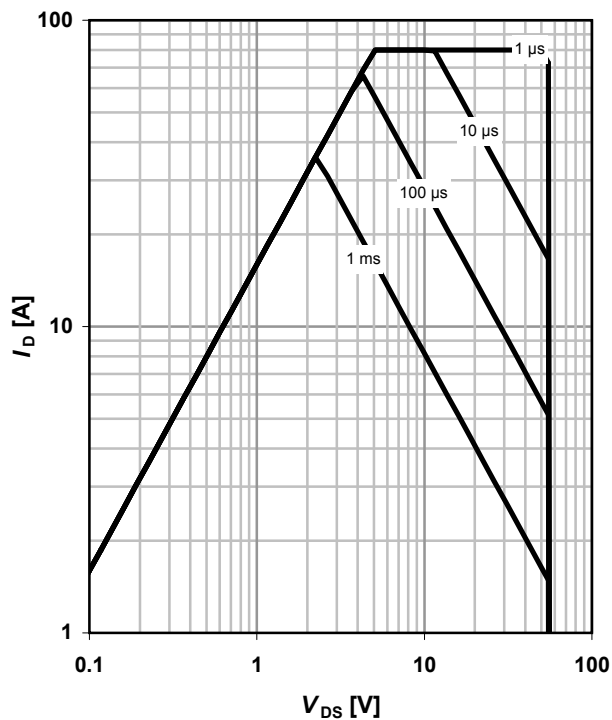
2 Drain current

$I_D = f(T_C)$; $V_{GS} \geq 6\text{ V}$; one channel active



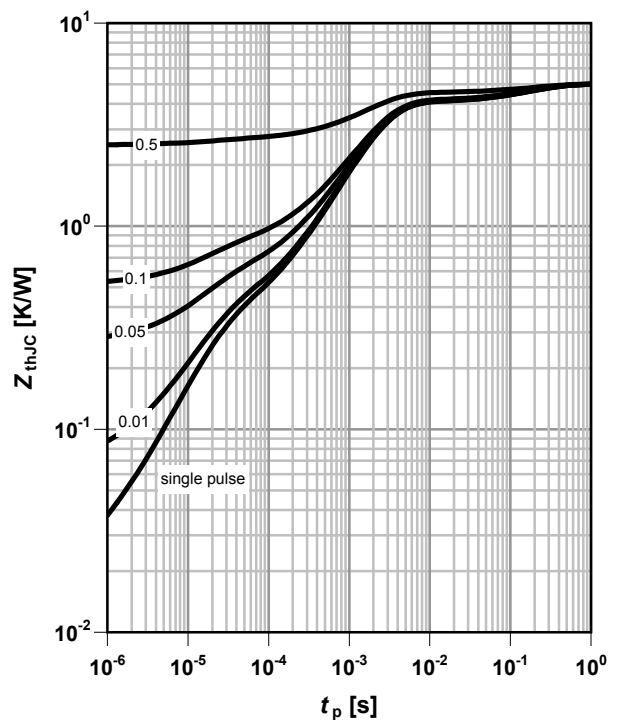
3 Safe operating area

$I_D = f(V_{DS})$; $T_C = 25^\circ\text{C}$; $D = 0$; one channel active
parameter: t_p



4 Max. transient thermal impedance

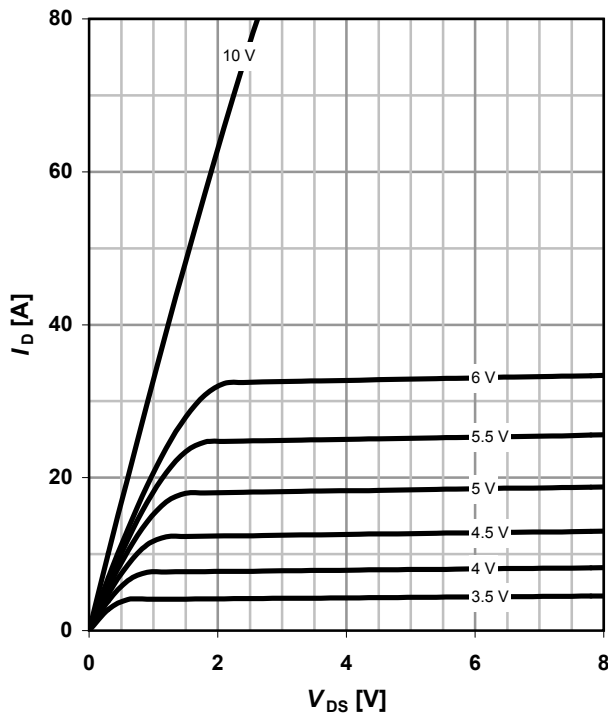
$Z_{thJC} = f(t_p)$
parameter: $D = t_p/T$



5 Typ. output characteristics⁵⁾

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

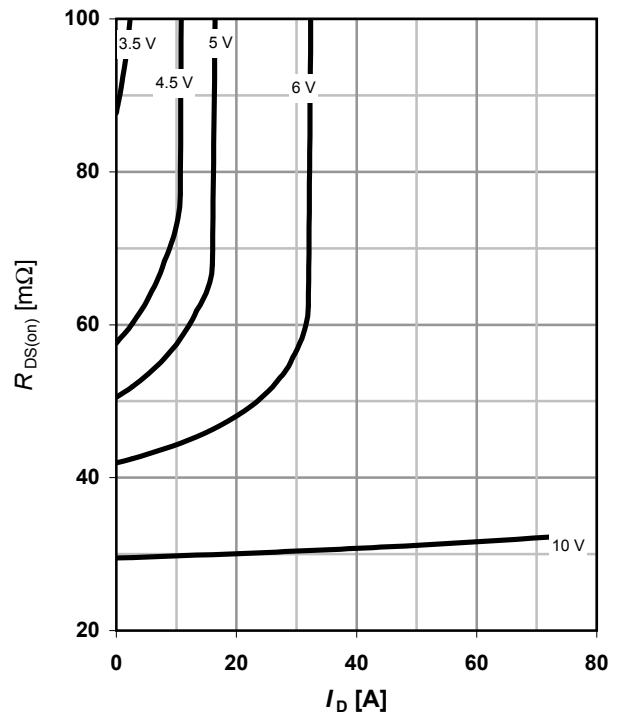
parameter: V_{GS}



6 Typ. drain-source on-state resistance⁵⁾

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

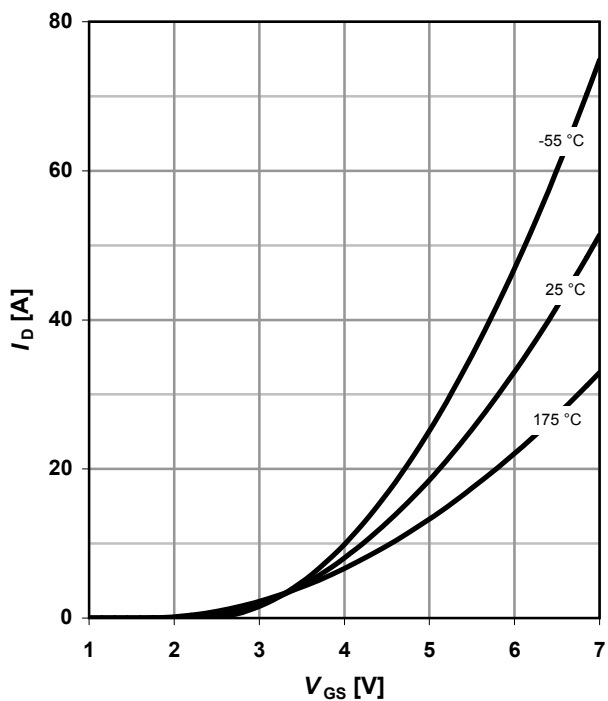
parameter: V_{GS}



7 Typ. transfer characteristics⁵⁾

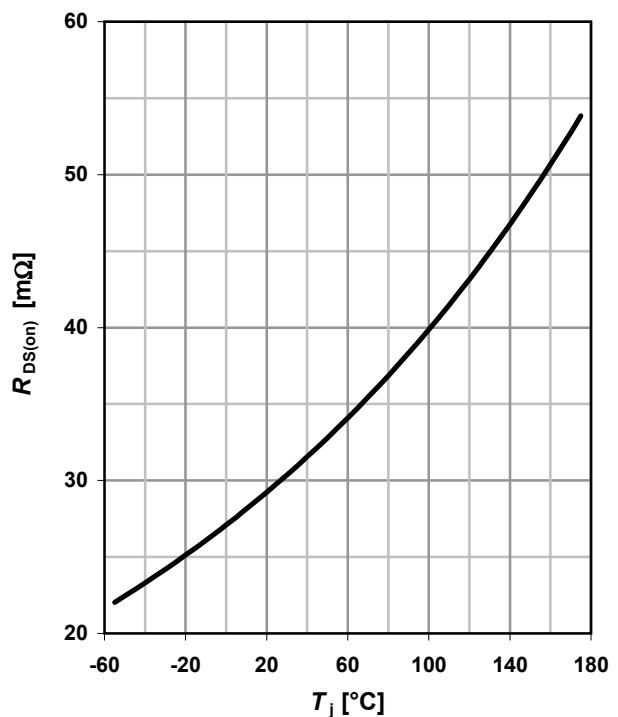
$I_D = f(V_{GS}); V_{DS} = 6V$

parameter: T_j



8 Typ. drain-source on-state resistance⁵⁾

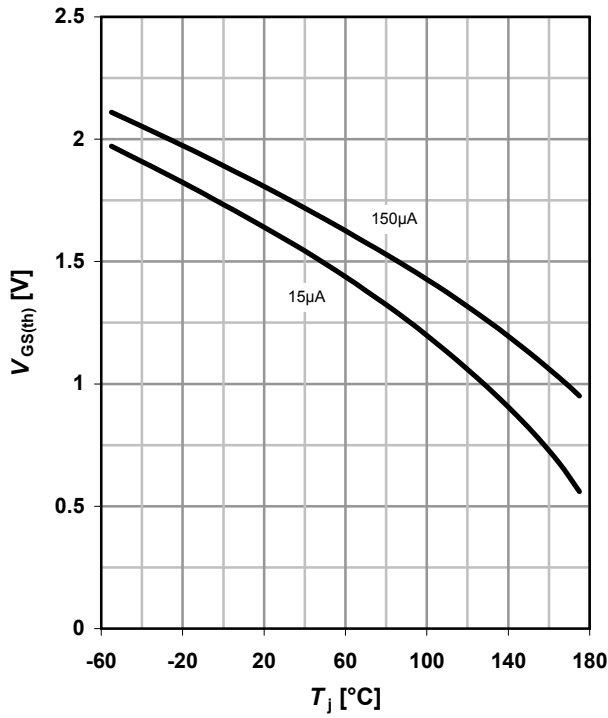
$R_{DS(on)} = f(T_j); I_D = 11\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

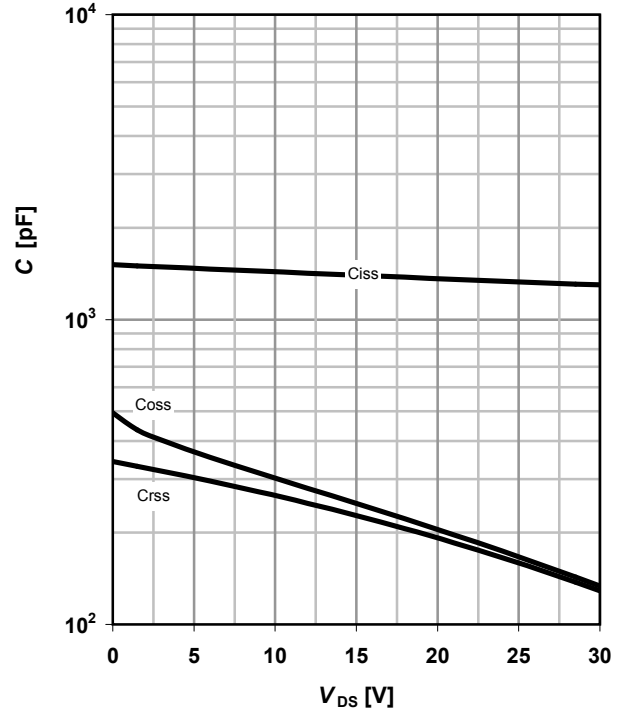
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. Capacitances⁵⁾

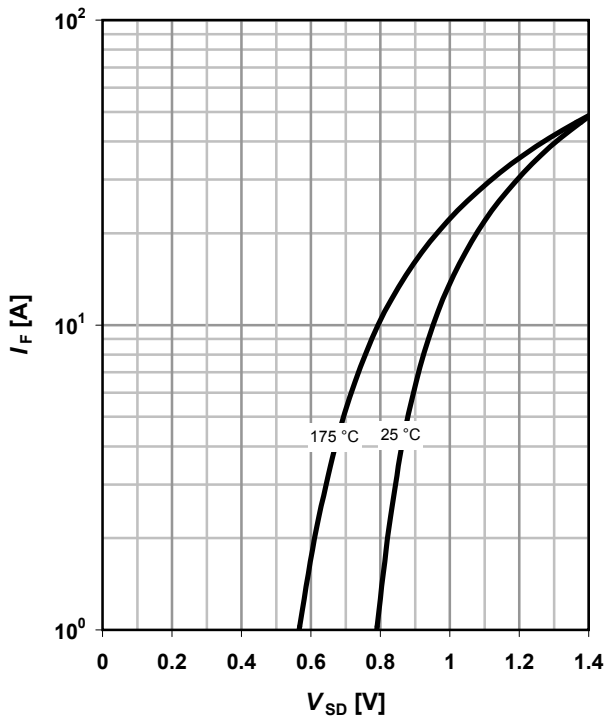
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics⁵⁾

$I_F = f(V_{SD})$

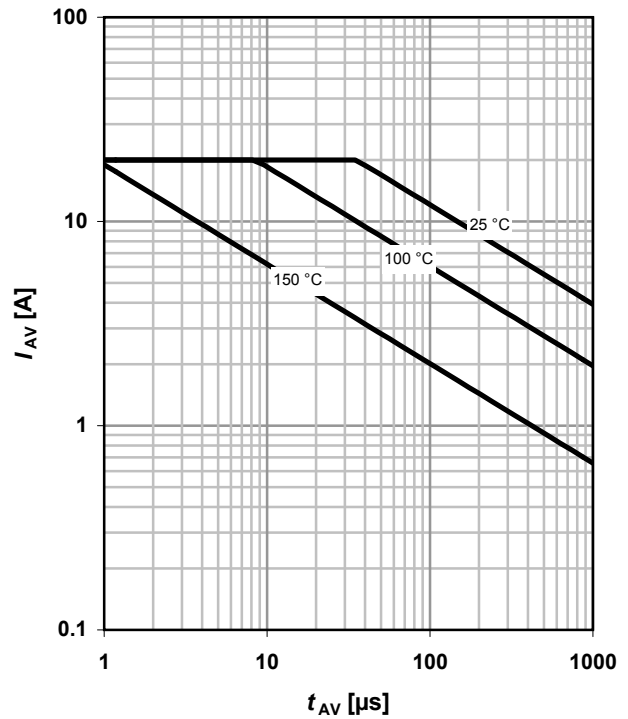
parameter: T_j



12 Avalanche characteristics⁵⁾

$I_{AS} = f(t_{AV})$

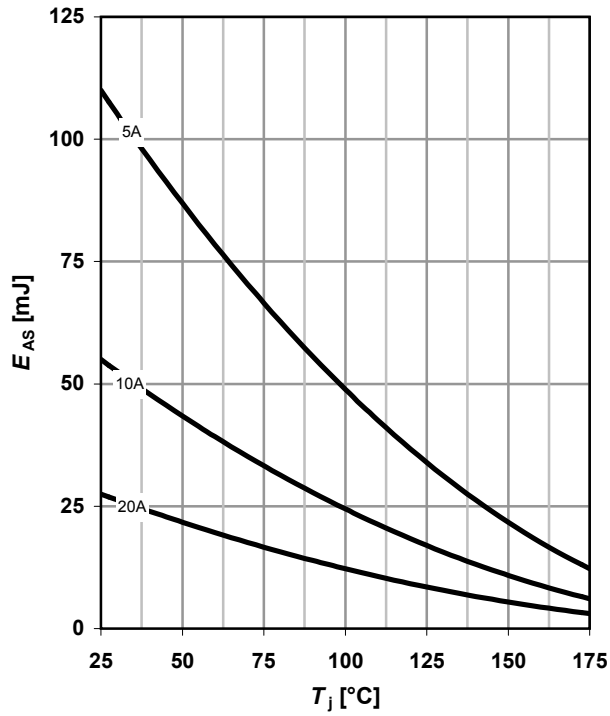
parameter: $T_{j(start)}$



13 Avalanche energy⁵⁾

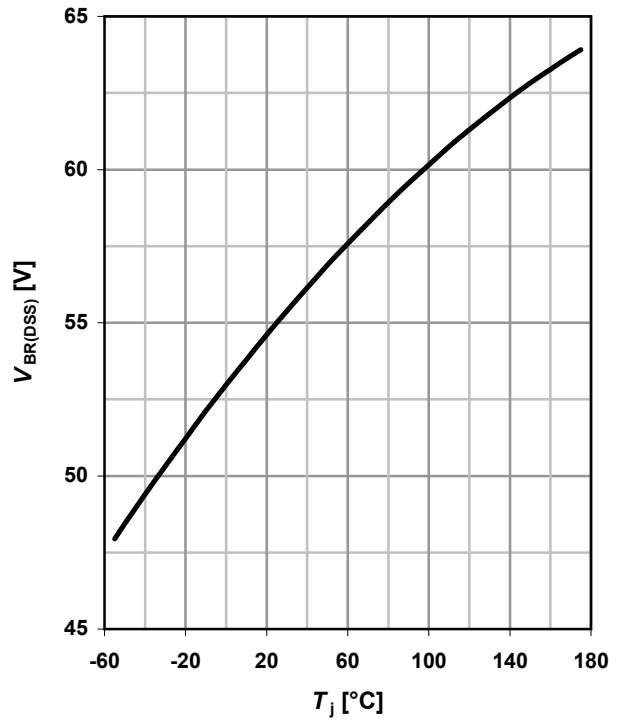
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

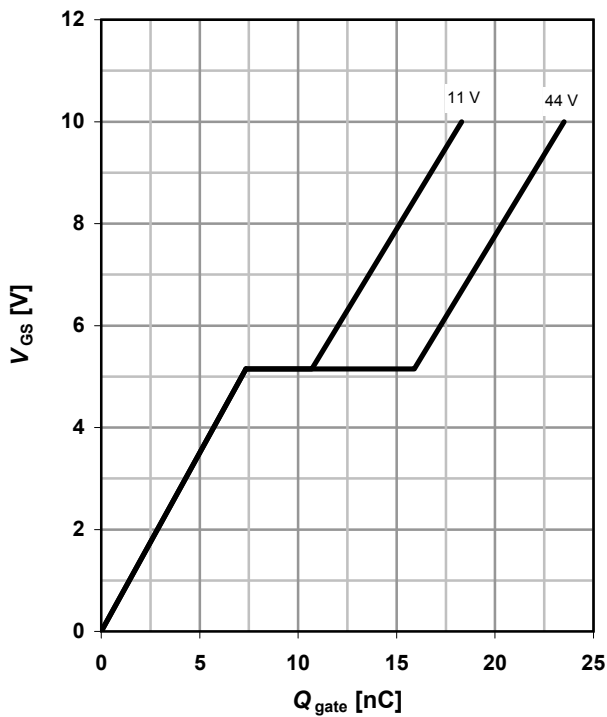
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



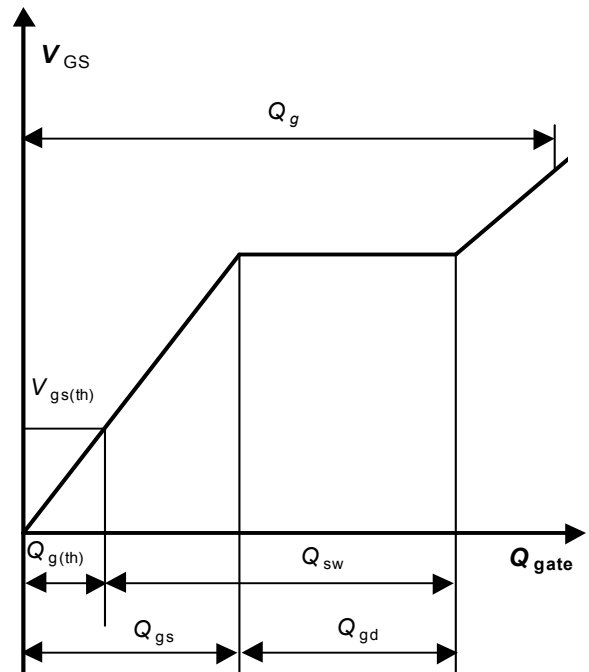
15 Typ. gate charge⁵⁾

$$V_{GS} = f(Q_{gate}); I_D = 20 \text{ A pulsed}$$

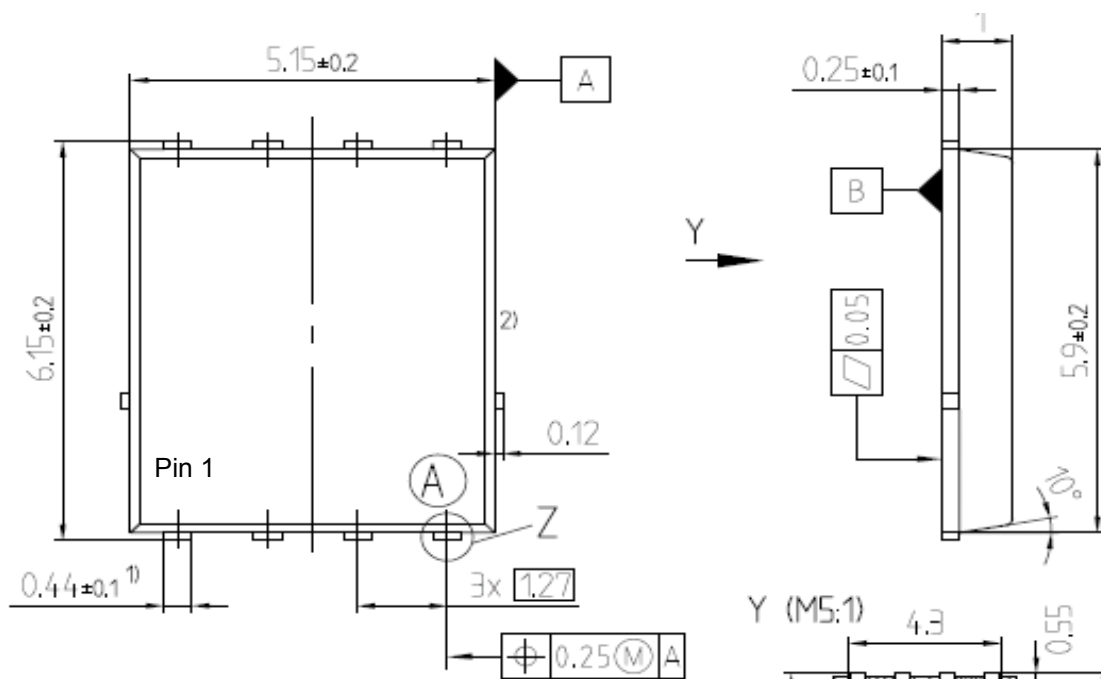
parameter: V_{DD}



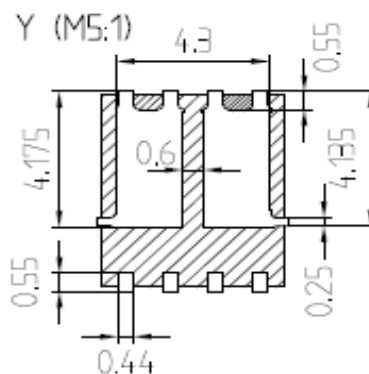
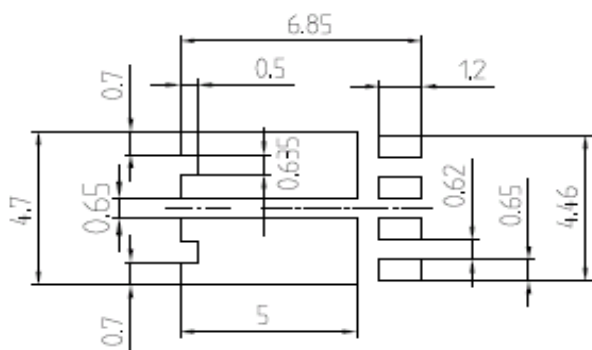
16 Gate charge waveforms



Package Outline



Footprint
(M5:1)



NOTE:

- ¹⁾ exclude mold flash
 - ²⁾ Removal on mold gate, intrusion 0.1mm
protrusion 0.1mm
- all metal surfaces: NiNiP plated

Dimensions in mm

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Revision History

Version	Date	Changes
Revision 0.1	08.12.2007	Initial Target Data Sheet
Revision 0.2	07.04.2008	Update of disclaimer, package drawing, layout according latest disclaimer
Revision 0.2	07.04.2008	Update of capacitances
Revision 0.2	07.04.2008	Condition Id Ron 5V and 10V updated
Revision 0.2	07.04.2008	Condition Id for Eas updated
Revision 0.3	04.05.2008	Initial Preliminary Data Sheet